

Designing high power efficient finite impulse response filters with three-four inexact adder-integrated Booth multiplier

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ABSTRACT

Finite impulse response (FIR) filters are widely utilized in several applications in digital signal processing, including data transmission, photography, digital audio, and biomedicine. It is necessary to use high sample rates for FIR filters, while moderate sample rates are needed for low-power circuits. To solve these problems, a Booth multiplier based on three-four inexact adder-based multiplication (TFIE-BM) was proposed. The goal of the proposed TFIE-based FIR Booth multiplier is to lower area usage, latency, and power consumption. The proposed method utilizes the spotted hyena optimizer (SHO) to find the optimal filter coefficient (FC) by minimizing the pass power consumption and Transition bandwidth. Moreover, a high-performance three-four inexact adder (TIFE adder) has been introduced, which uses fewer XOR gates for sum and carry generation, indicating that the logic has been simplified to reduce hardware complexity. By increasing speed and decreasing the FIR filter's critical path delay, a modified Booth multiplier that uses a 5:2 compressor is introduced. The overall delay of the proposed approach is 23.4%, 18.7%, 12.3%, and 5.7% lower than that of the Radix-4 Booth multiplier, CSA Booth multiplier, hybrid multiplier, and traditional Booth multiplier, respectively.

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1. INTRODUCTION

In the current generation, technology requires reducing the size of electronics equipment as well as enhancing of speed of devices [1]. Applications that make use of digital filters the most include those for image, video, and speech processing. Digital filters with finite impulse response (FIR) and infinite impulse response (IIR) are also available. Due to its superior stability and simple design, the FIR filter is suggested for the previously listed applications [2]. The linear phase property and robustness of FIR filters make them widely used in digital signal applications. Designing DSP systems requires a high-performance system; the most important factors are low power consumption and reduced clip size. FIR filters are crucial for image processing, mobile communications, and audio processing applications due to their inherent reliability and linear phase properties [3], [4]. In the present day, a number of FIR filter designs have been released, some for low-speed, some for high-speed, as well as others for low power consumption [5], [6].

Adder and multiplier circuits typically have the greatest impact on the delay and power performance of FIR filter designs. Multipliers typically dictate how long the FIR filter design takes to execute [7]. For the purpose of designing a delay with effective FIR filters, high-speed multipliers are therefore needed. The