

Performance Analysis of FinFET Based Digital Circuits

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Abstract. The scaling of the bulk MOSFETs has led to faster and denser integration of circuits. However, the downsizing is facing many challenges due to higher frequencies, lower supply voltages etc. in the nanometer regime due to the adverse short-channel effects. Those effects cause an increase in the leakage current, thus making circuits more sensitive to variations in process parameters. Thus, new options with much lesser short channel effects have been increasingly finding demand. Here in this paper, we discuss FinFET with 18 nm technology node, with the elevated conducting channel enabling the gate to surround it on three sides. Simulation studies of the 18 nm FinFET is done to analyse its static and transient performance parameters. The comparative performance analysis of the noise margins, delay and power of FinFET based inverter with that of a CMOS inverter using Cadence Virtuoso tool is discussed.

1. Introduction

Silicon based MOS Technology has been the very basis of Very Large Scale Integrated systems for many decades. According to Moore's law, the transistor size will be reduced by half in every 18 months. As the technology scales down, packing more transistors in unit chip area greatly enhances the SOC functionality [2]. Over a span of decades, semiconductor industry has been focusing primarily on CMOS technology scaling in order to reduce cost per function, increase speed and reduce power. CMOS scaling was initially accomplished by shrinking device physical feature sizes, in particular, gate-length and enabled by process innovations, such as scaled gate dielectrics, improved junction profiles, and new contact materials [1]. CMOS IC technologies have been scaled down continuously from long back and entered into the nanometer region.

As the technology scales down, the performance characteristics are degraded and the reliability of digital circuits against soft error and aging effects are reduced [3]. The design shrinking leads to many challenges and issues with the design like process variations, short channel effects and leakage currents etc. For these small dimensions, the systems has to suffer from many non-ideal effects like lowered trans-conductance, source to drain tunneling, gate oxide leakage, reduction in ON state current, mismatch in devices, fluctuations in doping patterns, degradation of mobility, delay problem etc. Such non-ideal effects result in increase of short channel effects which will rise exponentially leading to high power density and several variations in process. The scaling of CMOS devices has serious challenges due to the material and process limitations. In this regime, it is difficult to control the process parameters and cost shoots up for scaled devices Thus, shrinking scalability of MOSFETs is the main factor encouraging the scientists to