

Radix-8 Booth Encoded Approximate Multiplier Design for Energy-Efficient Image Processing Applications Using a 5:3 Compressor

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Abstract— Low-power design of the Arithmetic Logic Unit heavily relies on approximate computing. Applications involving image processing, like multimedia and signal processing, are its best fits. However, approximate computing is less accurate with area and power consumption. To overcome this, a novel high-performance multiplier architecture is proposed using Radix-8 Booth Encoding, and an approximate 5:3 compressor has been proposed. The proposed Radix-8 Booth encoding reduces the number of partial products. Signed bits of the multiplication are generated by grouping four multiplier bits using Radix-8 Booth encoding. Three bits are new bits and one is an overlapping bit at a time, and encodes them. The proposed 5:3 compressor efficiently compresses the partial product, leading to a reduced critical path and area. The proposed 5:3 compressor efficiently compresses five bits into three outputs, resulting in improved speed and reduced power consumption. By attaining high PSNR and MSSIM values, the proposed method is verified through image sharpening. Excellent image quality and structural similarity are provided by the high PSNR and MSSIM values. Using Xilinx ISE, the proposed multiplier is implemented on a 28 nm FPGA and assessed in terms of area, power, and delay. The proposed structure achieves up to 57% area, 51% power, and 40% delay reduction in comparison to existing approximate compressors and multipliers. Therefore, the proposed design is highly efficient for image-sharpening applications.

Keywords— Approximate computing, Radix-8 Booth encoding, Approximate compressor, low area, Image-sharpening

I. INTRODUCTION

The approximate computation reduces logic complexity at the expense of precision; it improves the functionality of existing digital logic systems or circuits [1]. An emerging method for designing Very Large-Scale Integration (VLSI) devices that use less energy is approximate computing [2]. It is also possible to use approximate computing for the various layers of abstraction. Adding potential errors to streamlining reasoning with a Karnaugh map can approximate computation at the logic level [3].

An essential arithmetic operation in fields like digital signal processing is multiplication. When multipliers are used, partial products are generated, and the final result is calculated via carry propagation [4]. Therefore, maintaining the multiplier's performance to remain competitive the multiplier requires increasing the speed [5].

An error-tolerant multiplier (ETM) divides the input operands into two groups: accurate and incorrect. Whereas non-multiplication is built with a specific number of errors in the inaccurate part, exact multiplication is carried out at higher order bits in the accurate part [6]. An approximate adder that can process data in parallel by severing the carry propagation chain is the first step in a fast multiplier. An approximate adder differs from an approximation adder primarily in that the latter adds multiple bits of the same significance, whereas the former adds two operands of multiple numbers of varying importance [7]. The already-existing approximate multipliers are more sophisticated and take up more space. The suggested approach thereby increases compression efficiency while lowering partial product complexity. The major contribution of the proposed work is given below:

- The proposed Radix-8 Booth encoding technique effectively minimizes hardware area and power consumption by reducing the number of partial product rows.
- Proposed 5:3 approximate compressor reduces complexity and enhances accuracy.
- The proposed compressor compresses five input bits into three output bits efficiently.
- Xilinx ISE 14.2 on 28 nm technology is used to synthesize the proposed design.
- The proposed design achieves high PSNR and MSSIM values in image sharpening.

This study report follows the following format. Section II provides an analysis of existing methods. Section III explains the proposed methods. Section IV provides a comprehensive analysis and discussion. Section V contains the conclusion.

II. LITERATURE

In 2021 Kumar, U.A et al., [8] proposed an unsigned approximation multiplier design to enhance hardware performance without sacrificing accuracy. The approximation error is compensated by a simple yet efficient error correction module. The most crucial component of the multiplier is implemented using exact logic since approximation will result in significant inaccuracy. Experimental results show that the 8-bit multiplier can reduce power and power-delay products by up to 47.7% and 55.2%, respectively.