Dr. KRISHNA KUMAR S.

Professor, Electronics and Communication Engineering

Administrative Responsibilities

- Head of the Department

Education Summary

- Ph.D in Thermal and Power-Aware Digital VLSI Testing from Indian Institute of Technology Kharagpur
- M.Tech in Computer Science and Engineering from Indian Institute of Technology Madras
- B.Tech in Electronics and Communication Engineering from T.K.M. College of Engineering, Kollam

Employment History

- Professor at Christ College of Engineering, Irinjalakuda. (July 2026 onwards)
- Professor at Federal Institute of Science and Technology, Angamaly. (July 2013 – June 2026)
- Associate Professor at Amrita Vishwa Vidyapeetham, Coimbatore. (May 1997 – June 2013)
- Lecturer (Project IMPACT) at Government Polytechnic College, Kalamassery. (June 1995 – April 1997)

Areas of Interest

1. CAD for VLSI
2. Computer Architecture
3. Embedded Systems
4. Digital Hardware Modelling
5. Design for Test and Testability

Specialised Training

- FDP on Real-Time and Embedded Systems at IIT Kharagpur from 19/09/2012 to 25/09/2012.
- FDP on Embedded Systems and Technology at IIT Kharagpur from 19/06/2006 to 24/06/2006.
- FDP on Embedded Systems and Technology at IIT Kharagpur from 19/06/2006 to 24/06/2006.
- FDP on Digital VLSI Frontend Design at IIT Madras from 06/09/2004 to 10/09/2004.
- FDP on Advanced Aspects of VLSI Design Automation at IIT Madras 13/09/2004 to 17/09/2004.
- FDP on Digital Circuit Testing and Design for Testability at VLSI Society of India, Bangalore from 17/08/2006 to 19/08/2006.
- FDP on Digital Electronics at NTTF Bangalore from 20/05/1996 to 07/06/1996.
- FDP on Introduction to Bio Information Algorithms and Their Parallel Implementations at Amrita Vishwa Vidyapeetham, Coimbatore from 10/11/2003 to 21/11/2003.
- FDP on Analog Electronics II at IIT Delhi from 30/10/1995 to 22/12/1995.
- Corporate Training on Tetramax (Tetramax – I Workshop) at Synopsys Bangalore from 22/12/2011 to 23/12/2011.
- Corporate Training on Design for Test Compiler (DFT Compiler) (DFTC – I Workshop) at Synopsys Bangalore from 19/12/2011 to 21/12/2011.
- Corporate Training on IUS, RTL Compiler at Cadence Bangalore from 12/02/2007 to 15/02/2007.
- Corporate Training on SoC Encounter, Virtuoso at Cadence Bangalore from 20/08/2007 to 24/08/2007.
- Corporate Training on Blast Fusion, Blast Create, Blast Rail, Blast Plan at MAGMA Bangalore from 19/01/2004 to 23/01/2004.

Journals/ Papers published

- Customizing Completely Specified Pattern Set Targeting Dynamic and Leakage Power Reduction During Testing *by* S. Krishna Kumar, Subhadip Kundu, Santanu Chattopadhyay Integration, the VLSI Journal, Volume 45, Issue 2, March 2012, Pages 211–221.

- Particle Swarm Optimization Based Scheme for Low Power March Sequence Generation for Memory Testing by S. Krishna Kumar, S. Kaundinya, Santanu Chattopadhyay Asian Test Symposium, ATS 2010, Shanghai, China, pp.401-406 (2010).
- Particle Swarm Optimization based Vector Reordering for Low Power Testing by S. Krishna Kumar, S. Kaundinya, Subhadip Kundu, Santanu Chattopadhyay The Sec. Int. Conf. on Computing, Communication and Networking Technologies, ICCCNT 2010, Karur, India, pp.1-5 (2010).
- Customizing Pattern Set for Test Power Reduction via Improved X-identification and Reordering by S. Krishna Kumar, S. Kaundinya, Subhadip Kundu, Santanu Chattopadhyay 16th International Symposium on Low Power Electronics and Design 2010, ISLPD 2010, Austin, Texas, USA, pp.177-182 (2010).
- Test Power Reduction with Test-Time Trade-Off by Subhadip Kundu, S. Krishna Kumar, Santanu Chattopadhyay IEEE International Symposium on Circuits and Systems, ISCAS 2010, Paris, (2010).
- Test Pattern Selection and Customization Targeting Reduced Dynamic and Leakage Power Consumption by Subhadip Kundu, S. Krishna Kumar, Santanu Chattopadhyay Asian Test Symposium, ATS 2009, Taiwan, pp.307-312 (2009).
- Circuit Partitioning Using Particle Swarm Optimization for Pseudo- Exhaustive Testing by S. Krishna Kumar, P. Uday Bhaskar, Santanu Chattopadhyay, Pradip Mandal International Conference on Advances in Recent Technologies in Communication and Computing, ARTCom 2009, Kottayam, India, pp.346-350 (2009).
- Low Power Pseudoexhaustive Testing with Cellular Automata by S. Krishna Kumar, P. Uday Bhaskar, Santanu Chattopadhyay International Conference on Advances in Computing, Control, and Telecommunication Technologies, ACT 2009, Trivandrum, India, pp.419-423 (2009).